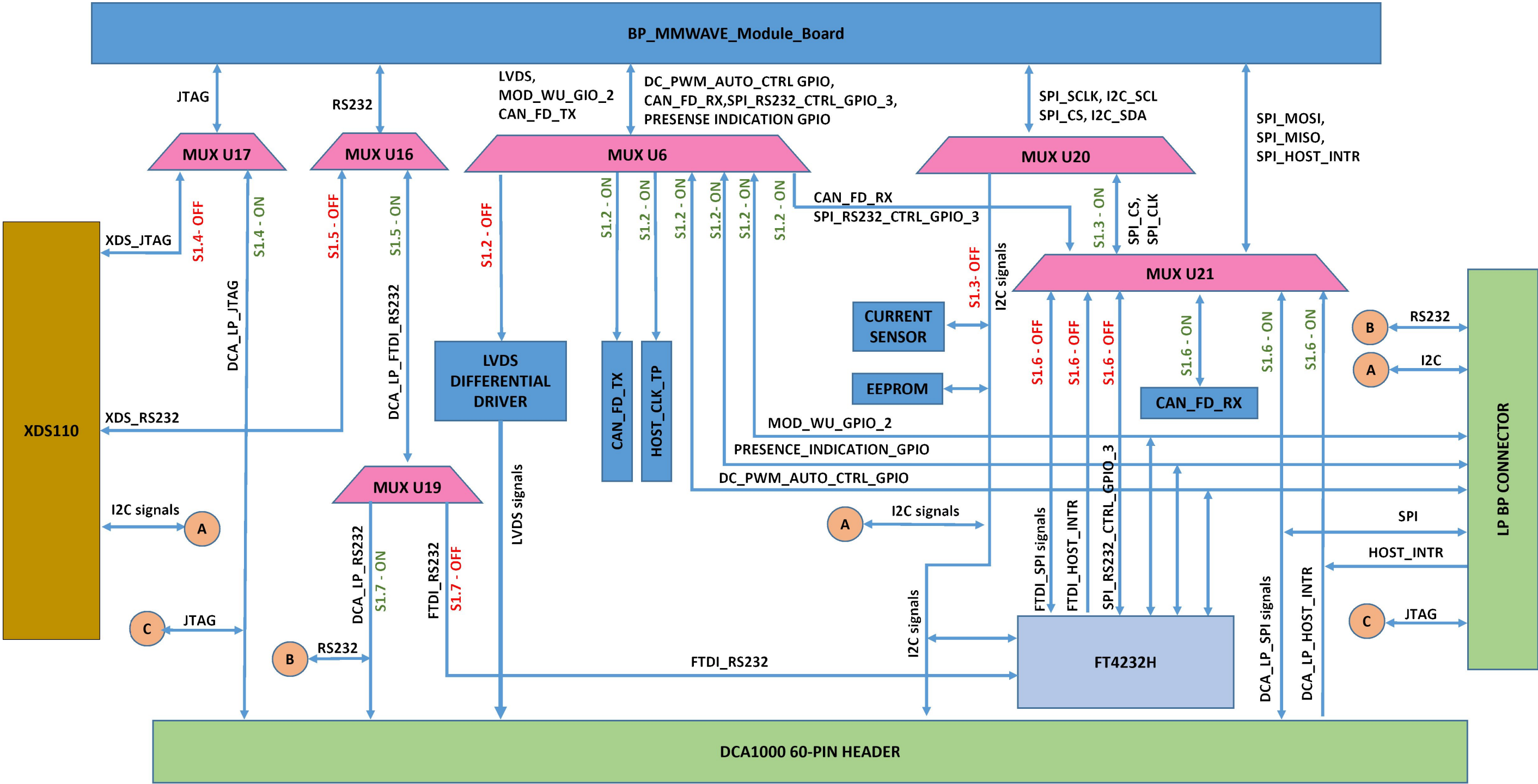




MUX BLOCK DIAGRAM



1	2	3	4	5	6
A					A
B					B
C					C
D					D

TABLE OF CONTENTS

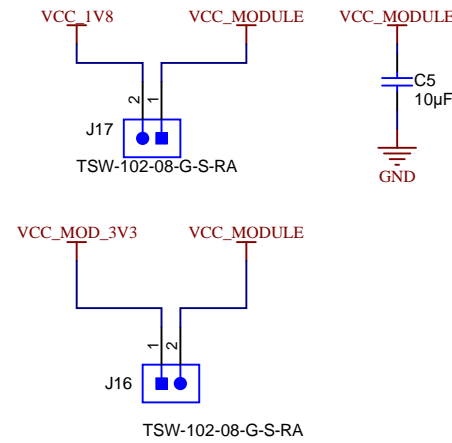
SHEET NO.	SHEET NAME
1	BLOCK DIAGRAM
2	MUX BLOCK DIAGRAM
3	TABLE OF CONTENTS
4	XWRL6432_MODULE_LGA
5	USB_DC_JACK_PWR_SWITCH
6	DC REGULATORS_LDOs
7	ANALOG_MUX_LVDS_DRIVER
8	ANALOG_MUX_SPI
9	ANALOG_MUX_JTAG, CAN & SOP_CTRL
10	CURRENT_SENSORS_EEPROM
11	XDS110_INTERFACE
12	FTDI_INTERFACE
13	RESET_SW_PRESENCE IND. LEDs
14	DCA1000_LP_BP_CONNs
15	EVM_HARDWARE

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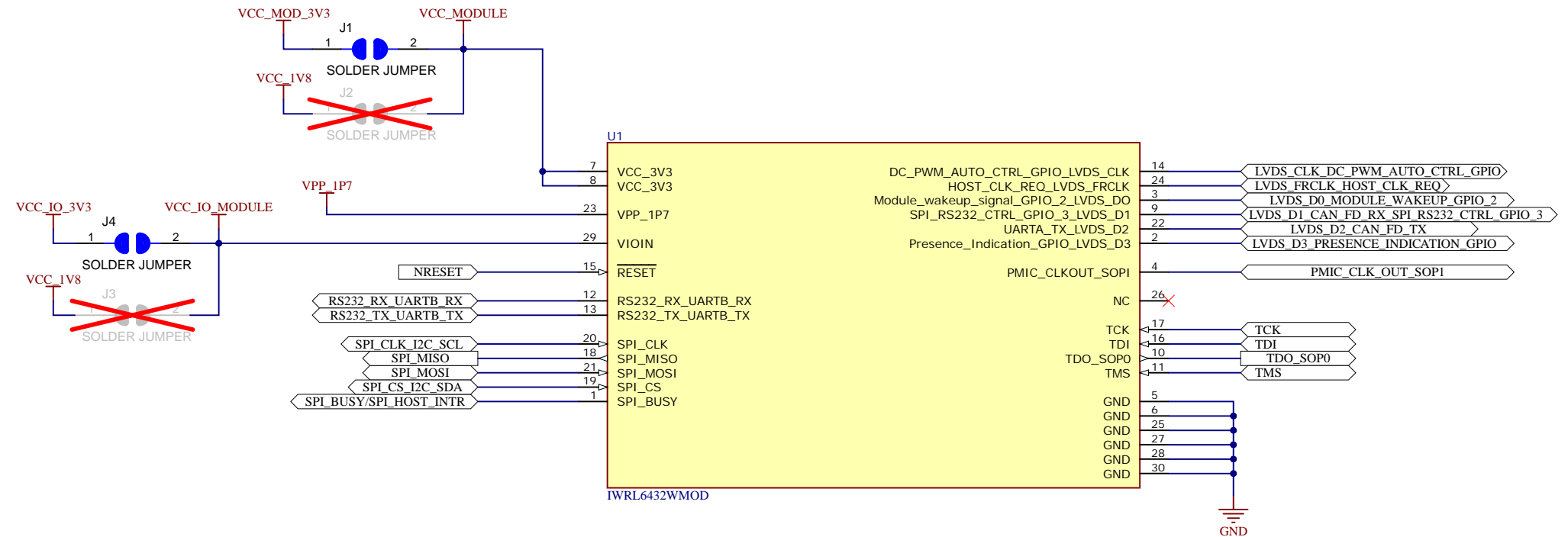


## BP\_MMWAVE\_MODULE

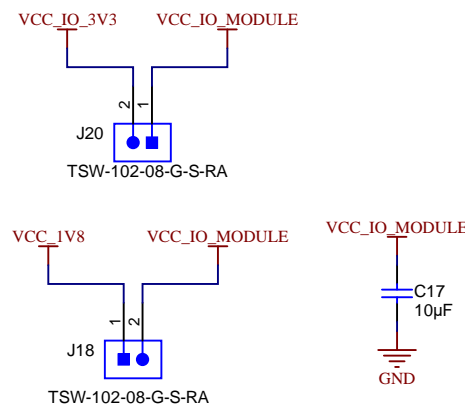
## 1.8V & 3.3V OPTIONAL MODULE SUPPLY



Design Note: Do not Plug in J17 and J16 at same time

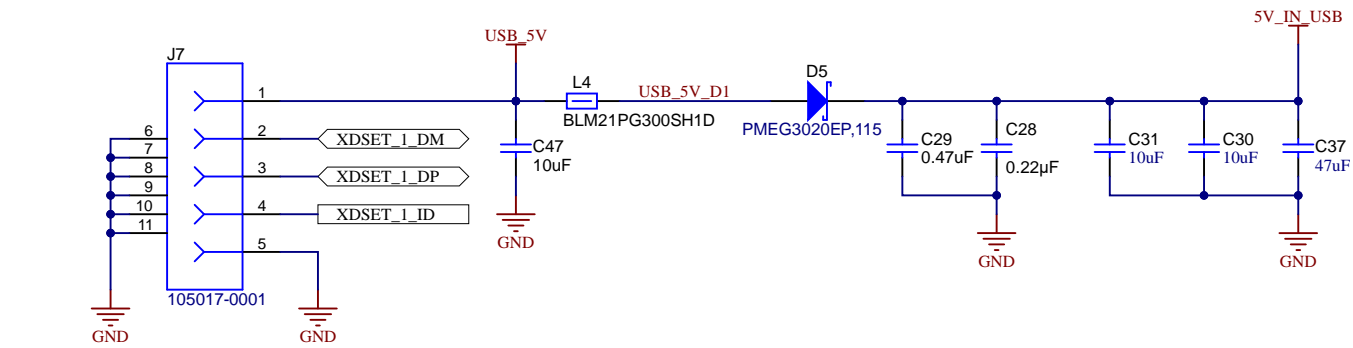


## 1.8V & 3.3V OPTIONAL MODULE I/O SUPPLY

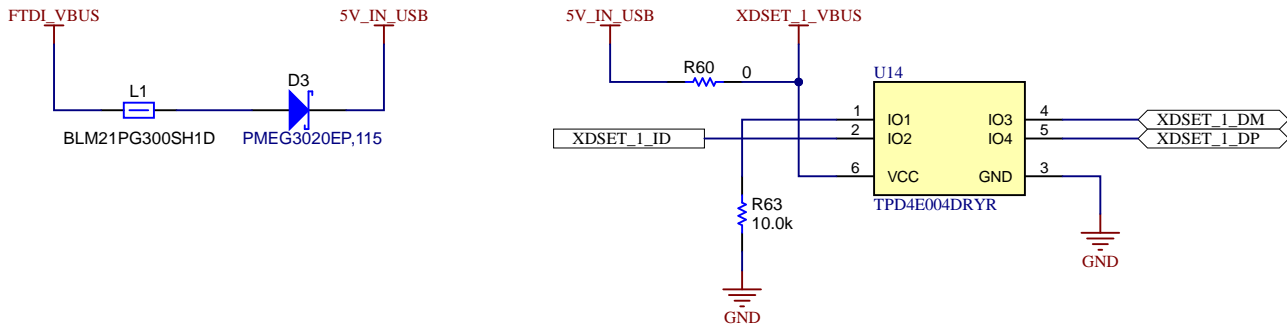


Design Note: Do not Plug in J18 and J20 at same time

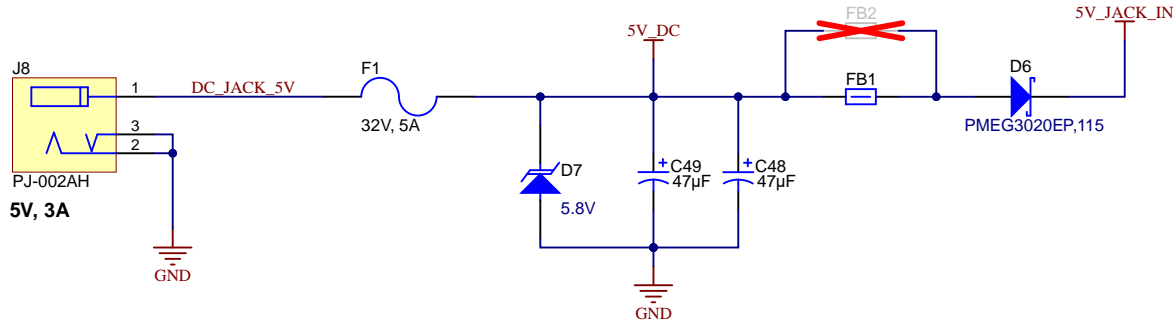
USB CONNECTOR



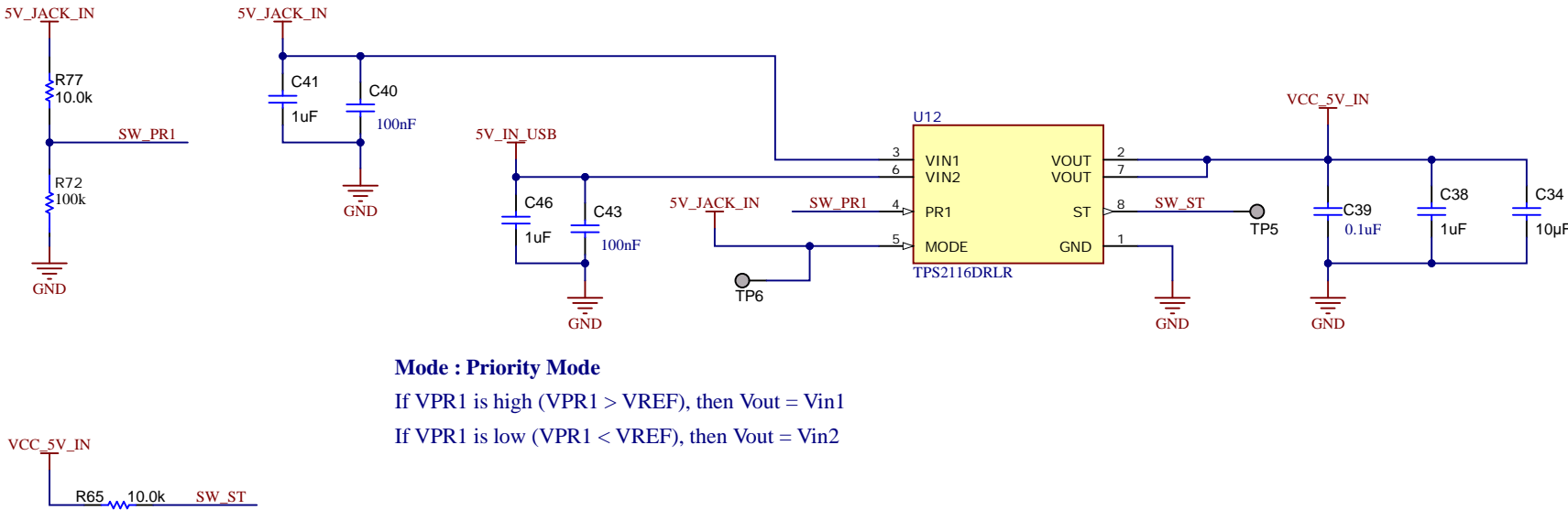
ESD DIODE



DC JACK



POWER LOAD SWITCH

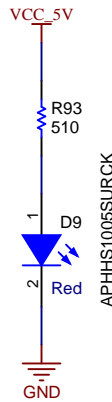


Mode : Priority Mode

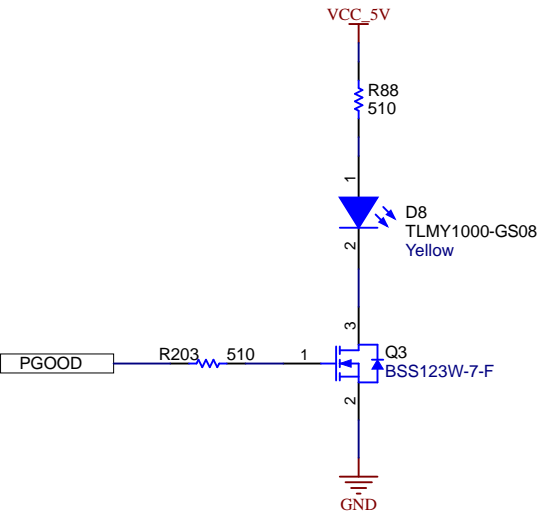
If VPR1 is high (VPR1 > VREF), then Vout = Vin1

If VPR1 is low (VPR1 < VREF), then Vout = Vin2

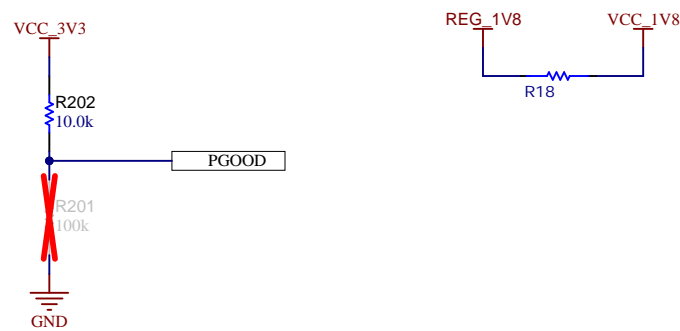
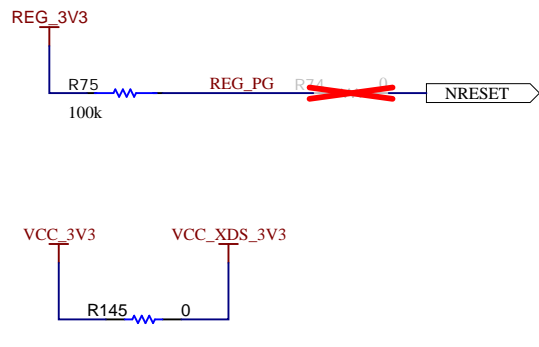
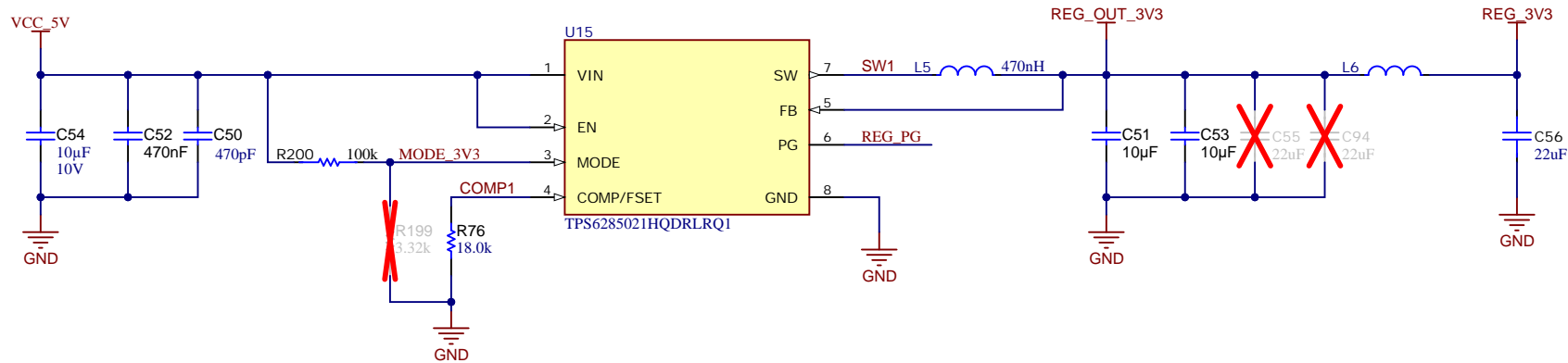
5V LED INDICATION



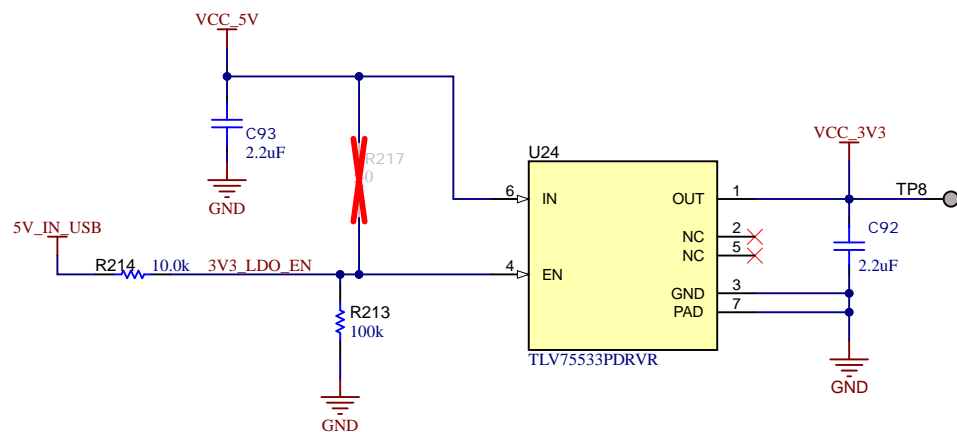
PGOOD LED



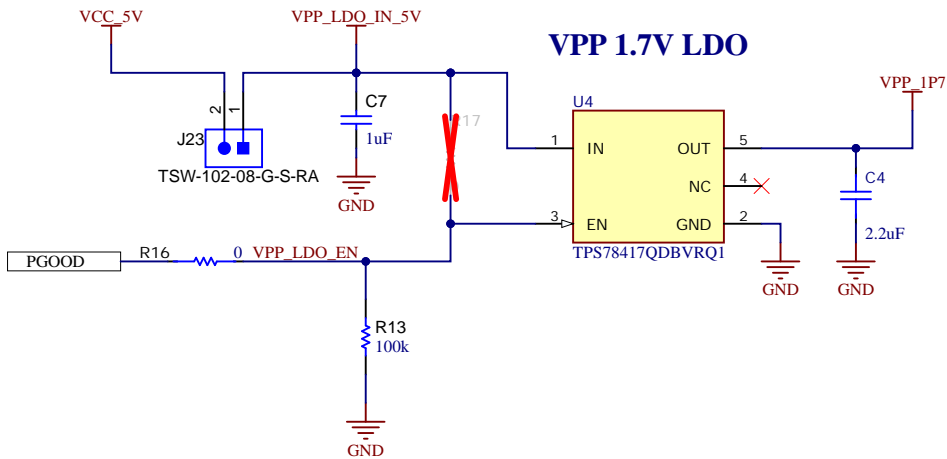
DC DC REGULATOR - 3.3V



LDO - 3.3V



VPP 1.7V LDO

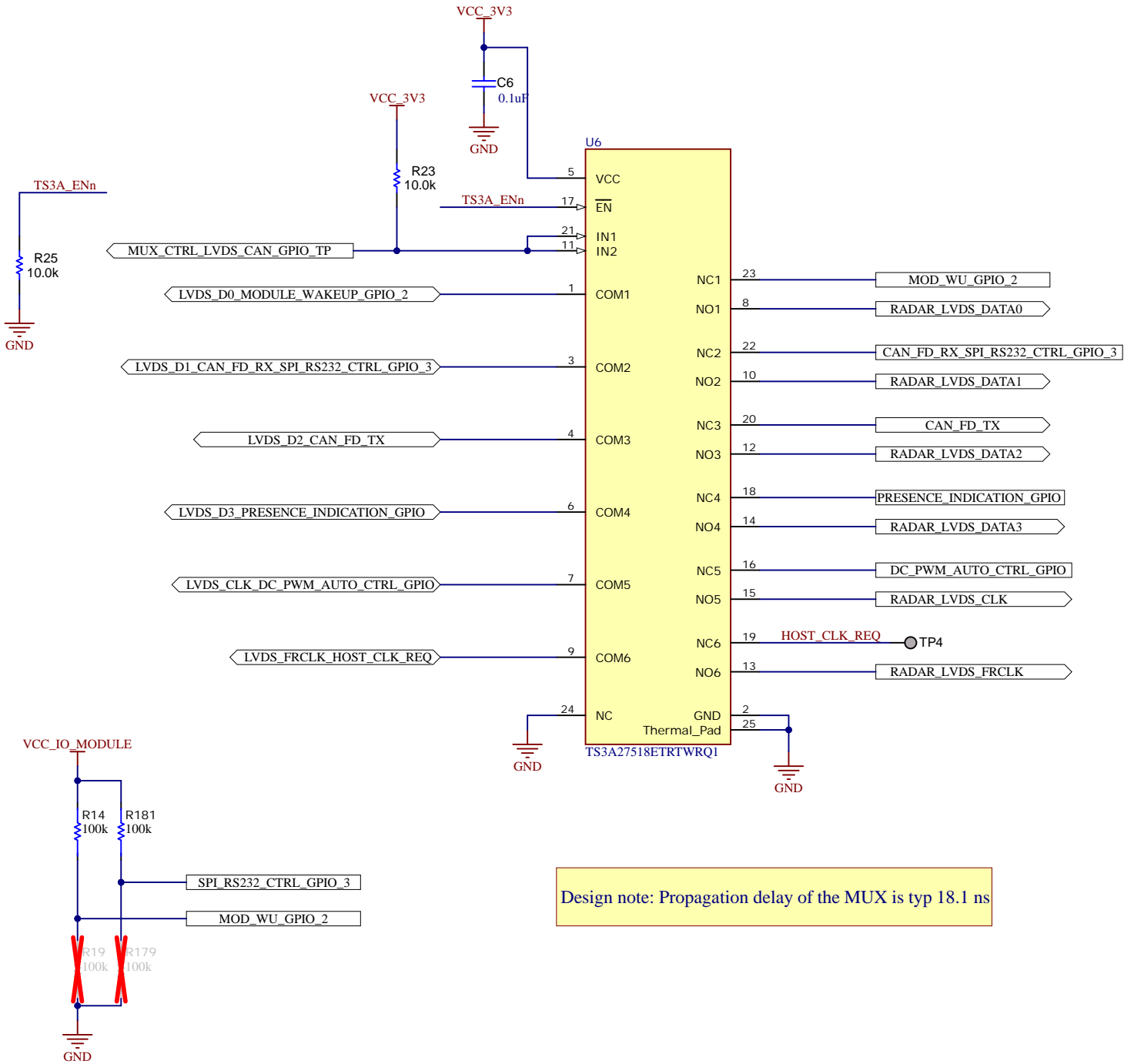


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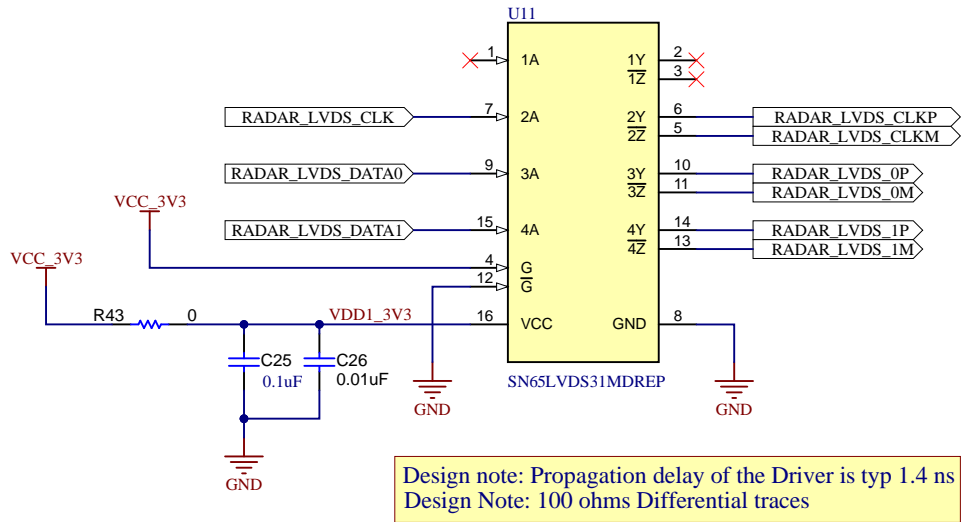
Orderable: BP-IWRL6432WMOD	Designed for: Public Release	Mod. Date: 22-10-2025
TID #: N/A	Project Title: BP-IWRL6432WMOD	
Number: PROC212	Rev: A	Sheet Title: DC REGULATOR LDO SECTION
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 6 of 15
Drawn By: Mistral	File: PROC212A_DC_Regulators.SchDoc	Size: B
Engineer: Mistral	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



ANALOG MUX - LVDS, UARTA

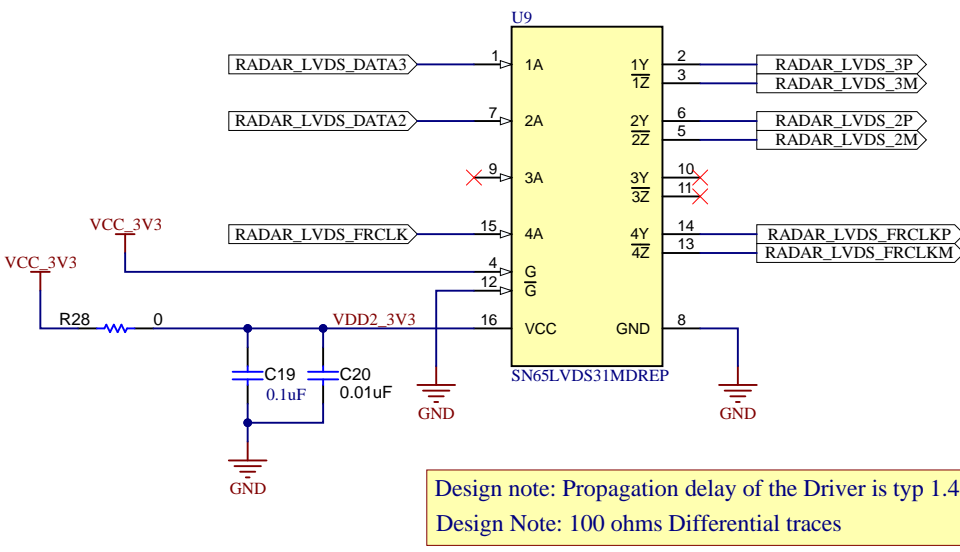


DIFFERENTIAL LVDS DRIVER



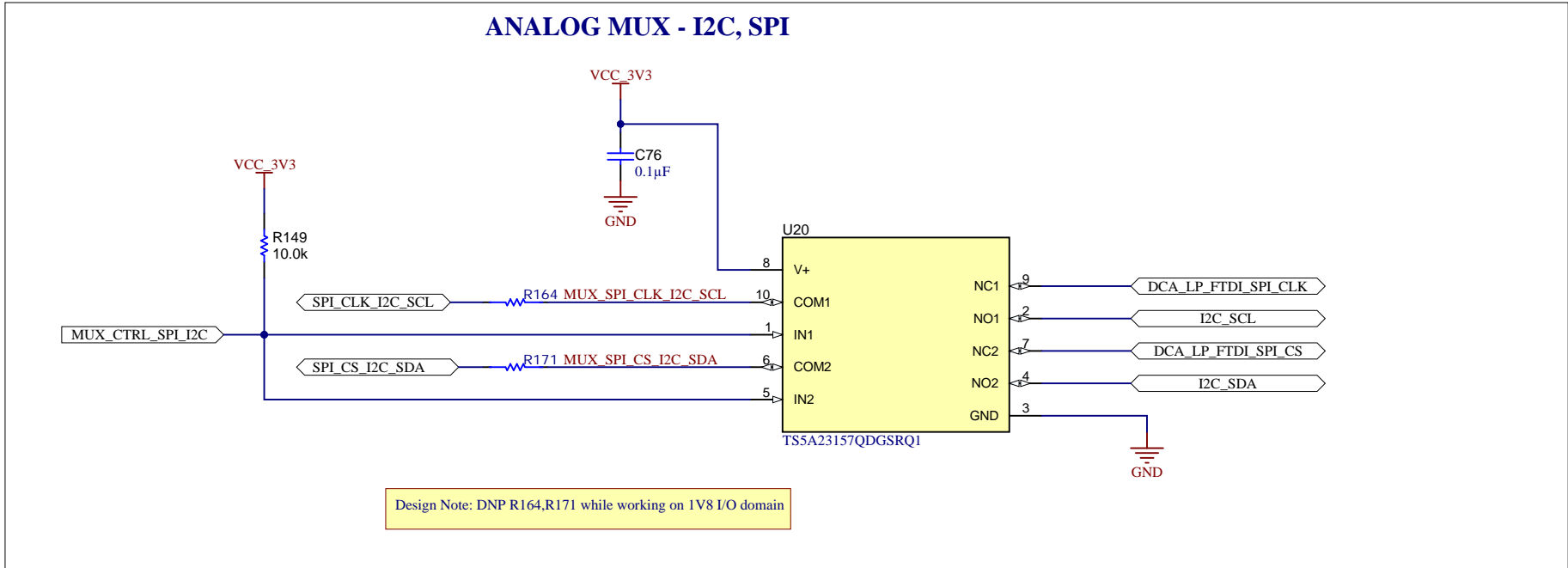
Design Note: The LVDS interface is mainly for evaluation purpose. Module software may not support LVDS

DIFFERENTIAL LVDS DRIVER

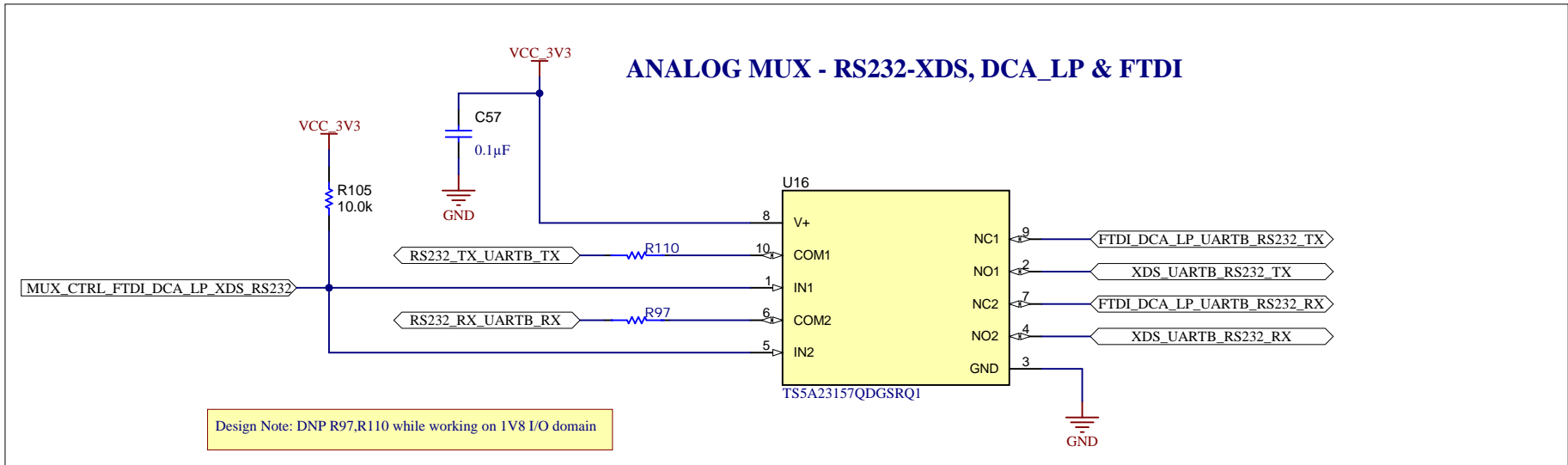


Design Note: The LVDS interface is mainly for evaluation purpose. Module software may not support LVDS

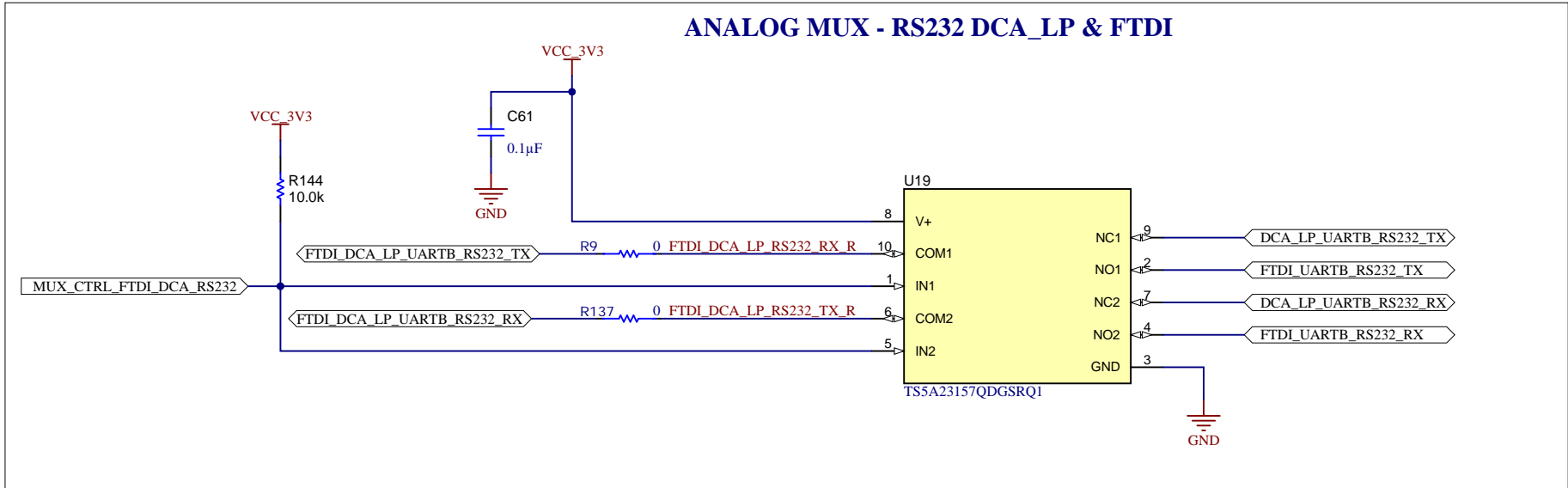
A



B

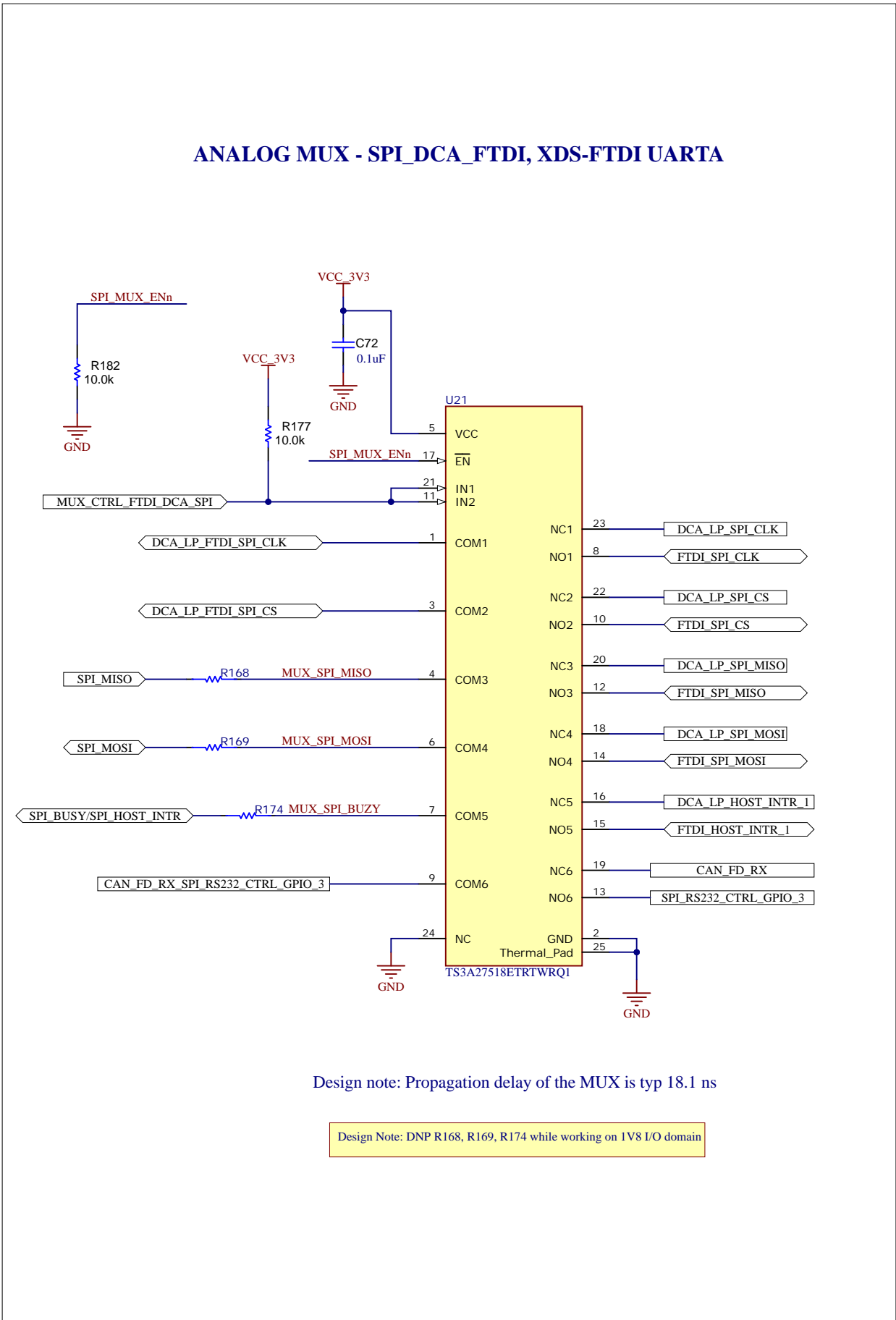


C



D

A

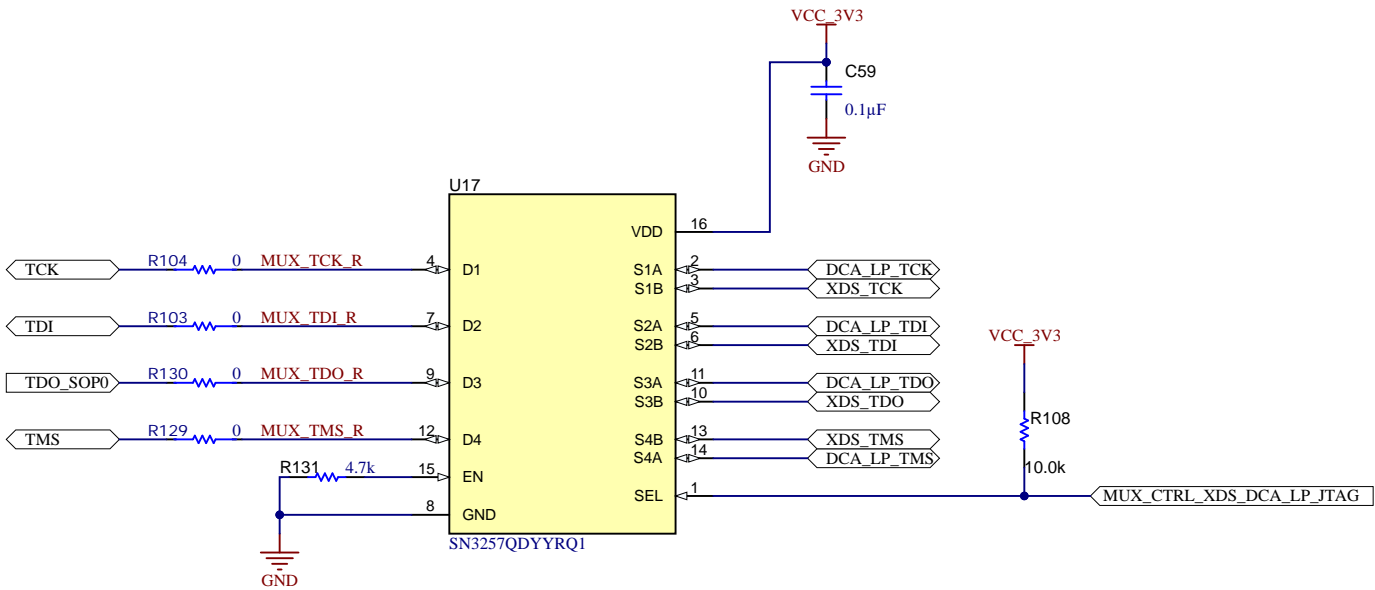


B

C

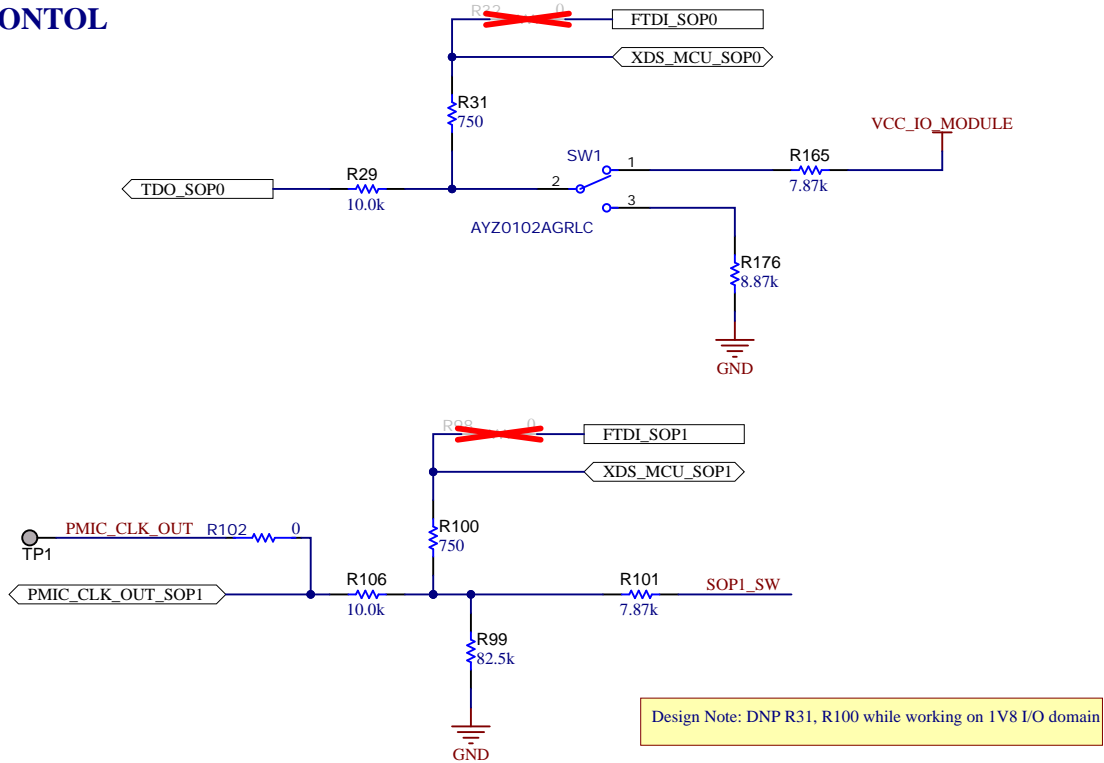
D

ANALOG MUX - JTAG



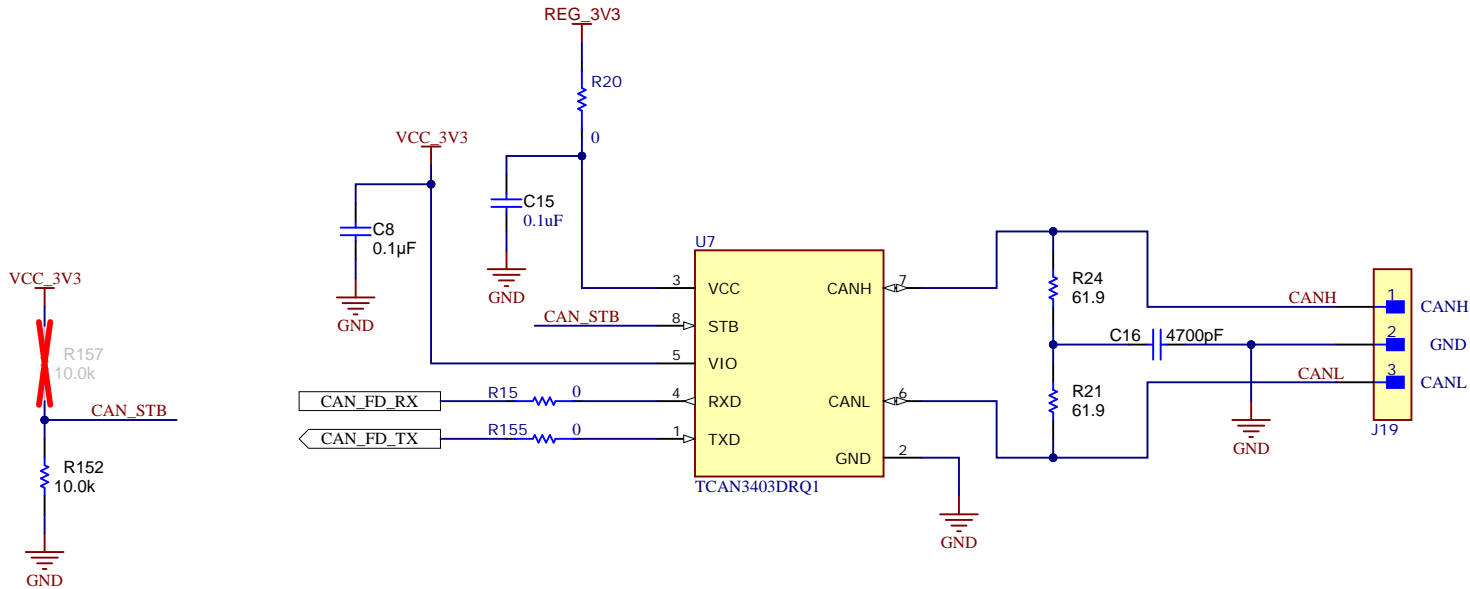
Design Note: DNP R104,R103,R130,R129 while working on 1V8 I/O domain

SOP CONTOL



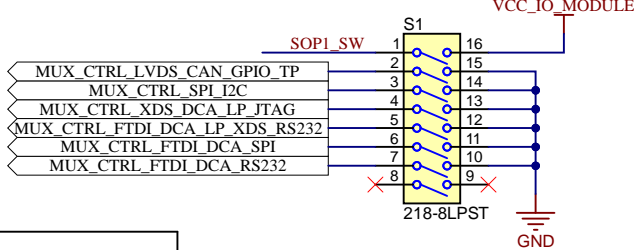
SOP CONFIGURATION			SWITCH POSITION	
SOP Mode	PMIC_CLK_OUT, TDO	Combination	S1.1(SOP1)	SW1(SOP0)
SOP_MODE1	Device management mode / QSPI Flashing mode	0 0	OFF	2-3
SOP_MODE2	Application mode / Functional mode	0 1	OFF	2-1
SOP_MODE4	Debug mode / mmWave studio connectivity mode	1 1	ON	2-1

CAN\_TRANCEIVER



Design Note: Mount R157 & DNP R152 for Standby mode. TCAN is configured in normal mode by default.

MUX CONTROL SWITCH



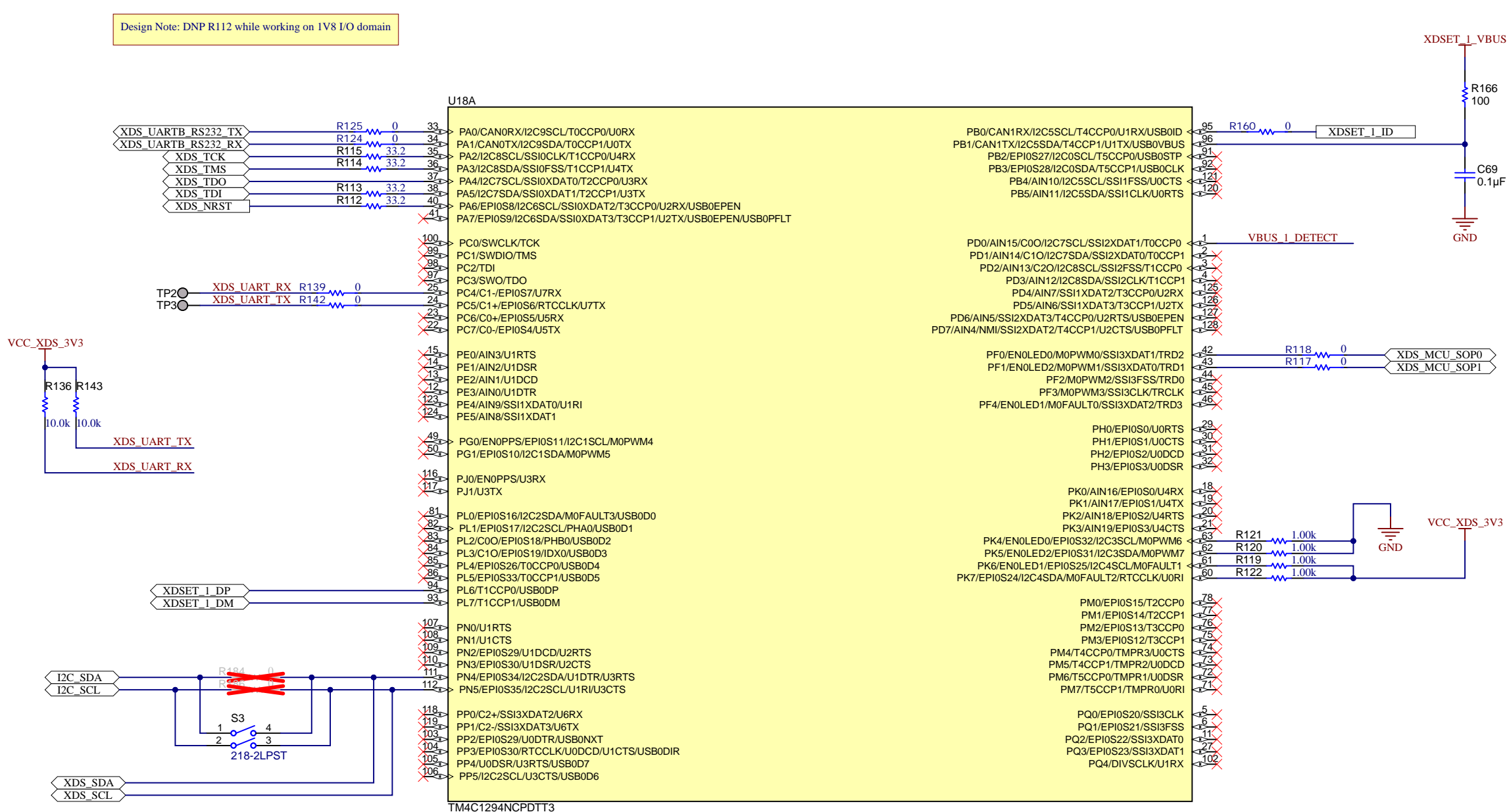
MUX TABLE

	Switch Position OFF	Switch Position ON
S1.2	LVDS	MOD_WU_GPIO_2, SPI_RS232_CTRL_GPIO_3 PRESENSE_INDICATION_GPIO, CAN_FD_TX DC_PWM_AUTO_CTRL_GPIO, HOST_CLK
S1.3	I2C	DCA_FTDI_SPI_CLK, DCA_FTDI_SPI_CS
S1.4	XDS_JTAG	DCA_LP_BP_JTAG
S1.5	XDS_RS232	FTDI_DCA_LP_RS232
S1.6	FTDI_SPI SPI_RS232_CTRL_GPIO	DCA_LP_SPI CAN_FD_RX
S1.7	FTDI_RS232	DCA_LP_RS232

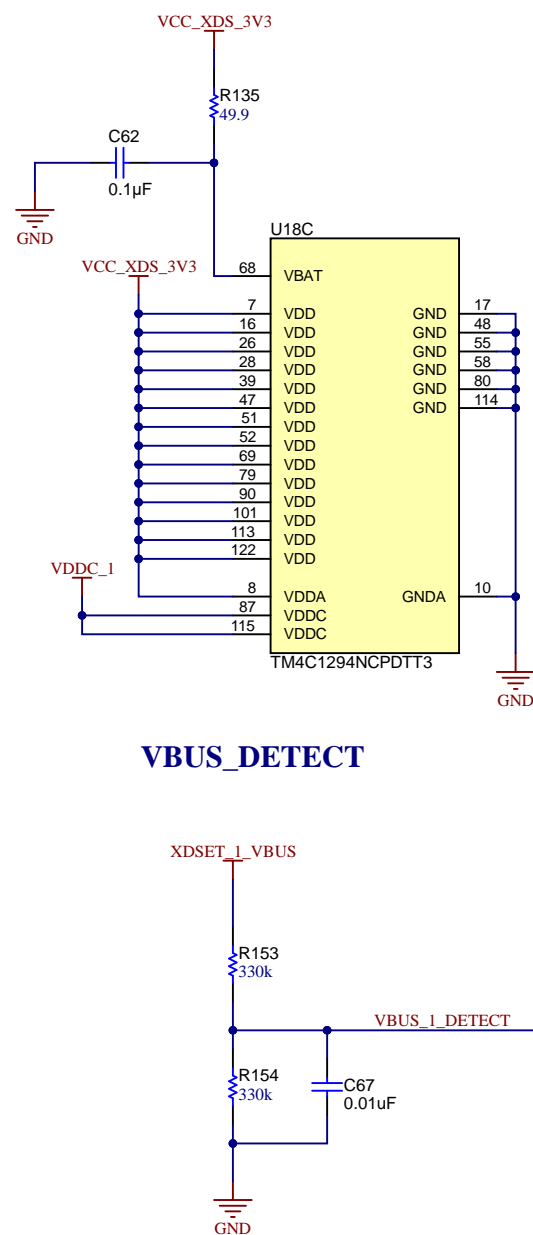


# XDS110

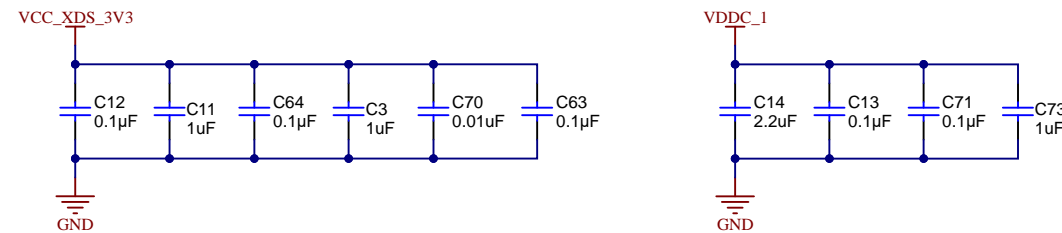
Design Note: DNP R112 while working on 1V8 I/O domain



## VBUS\_DETECT



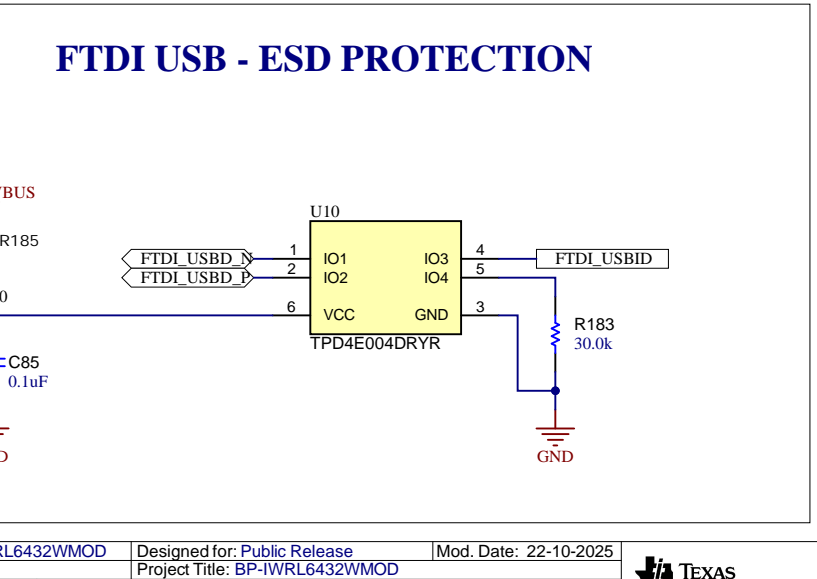
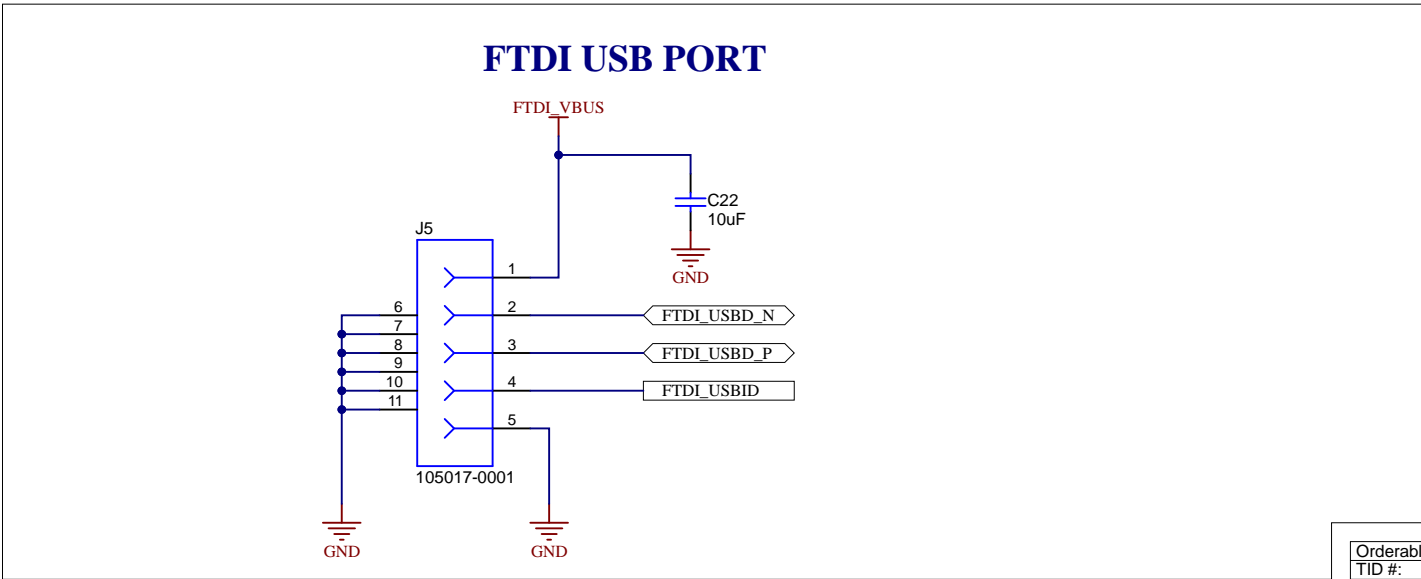
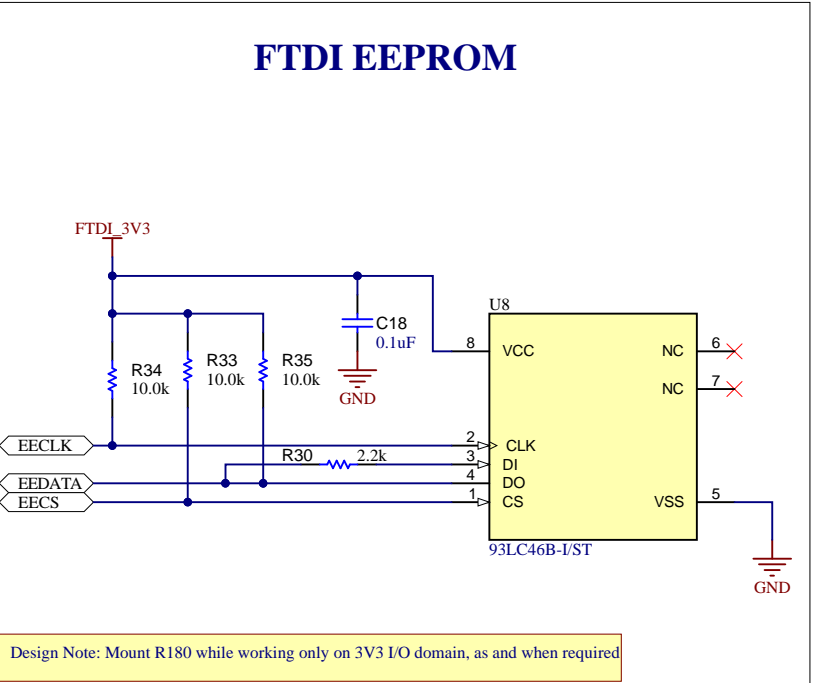
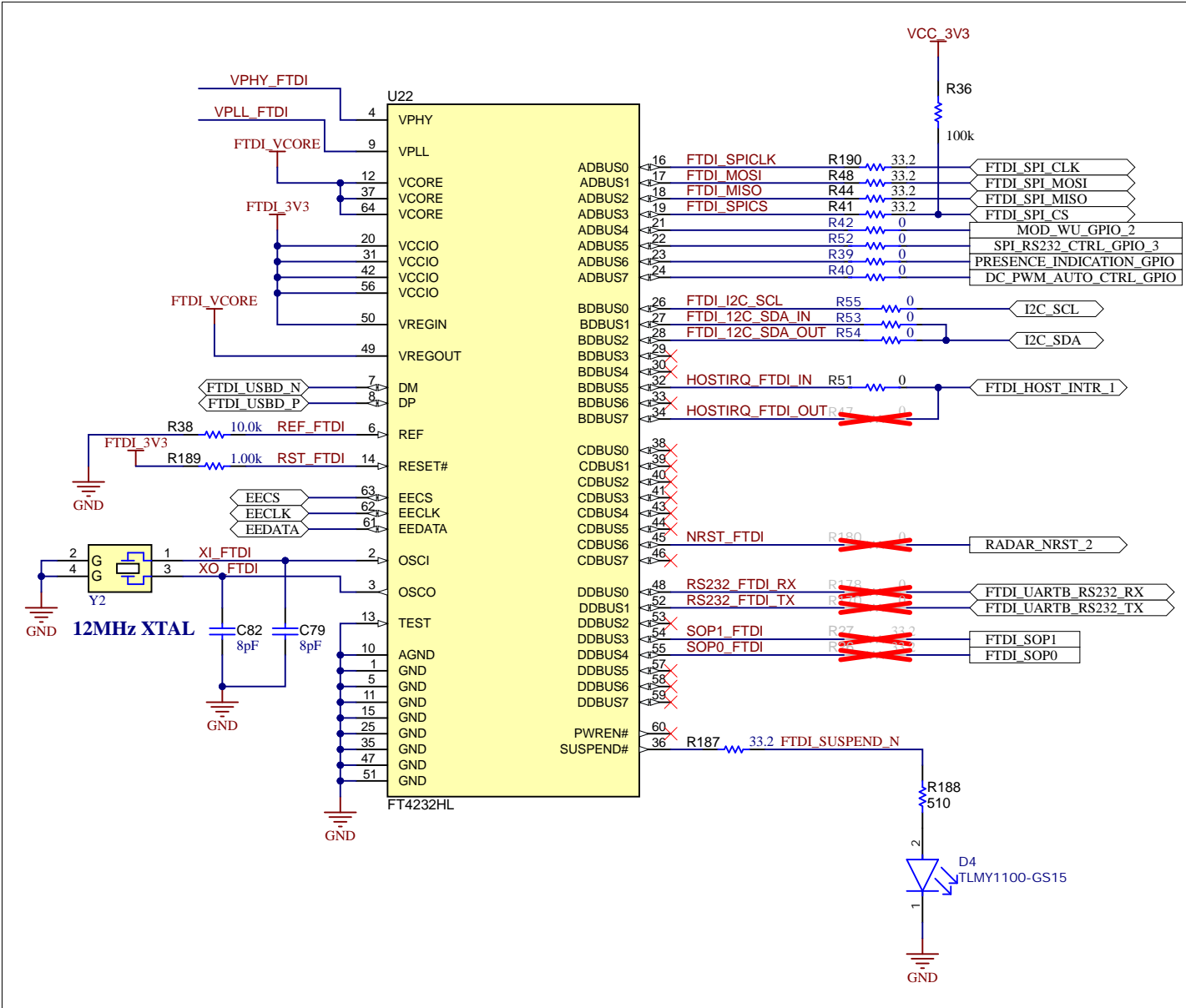
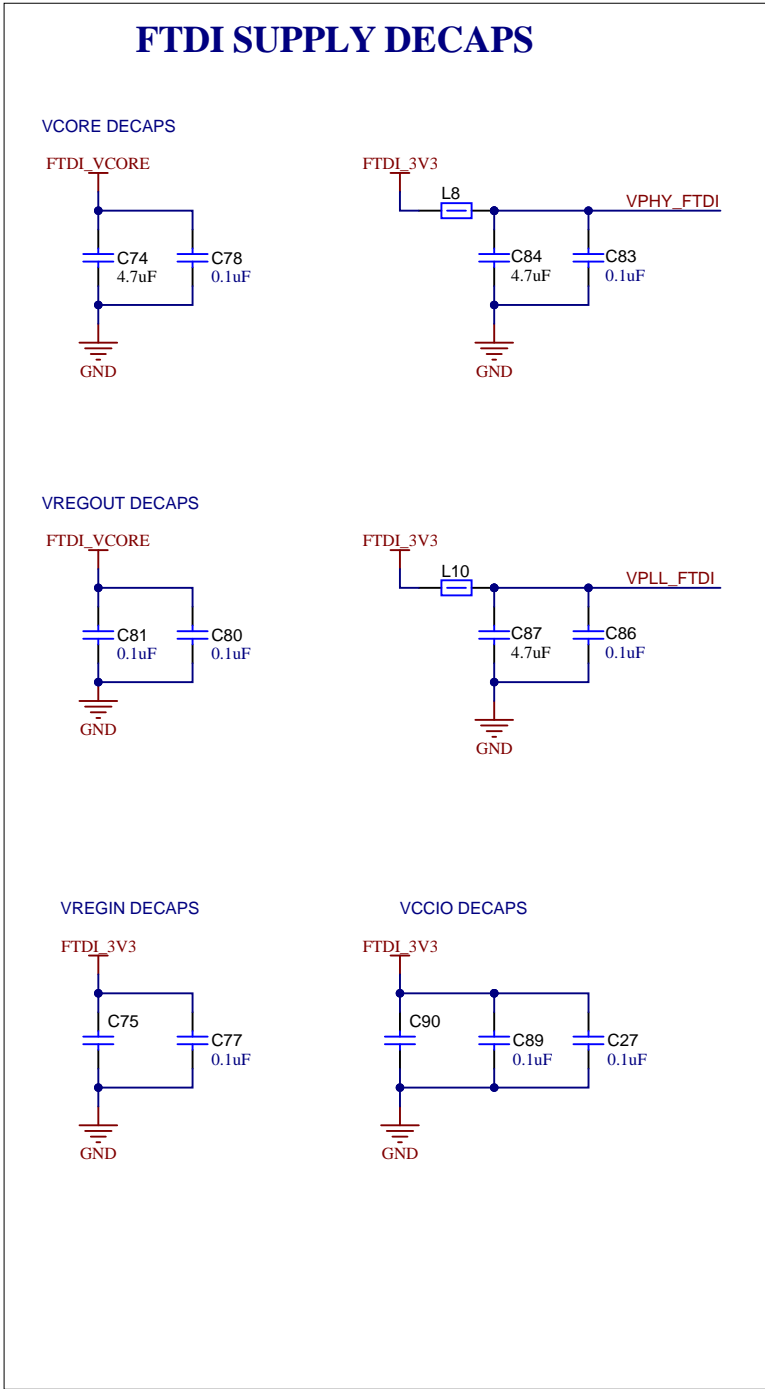
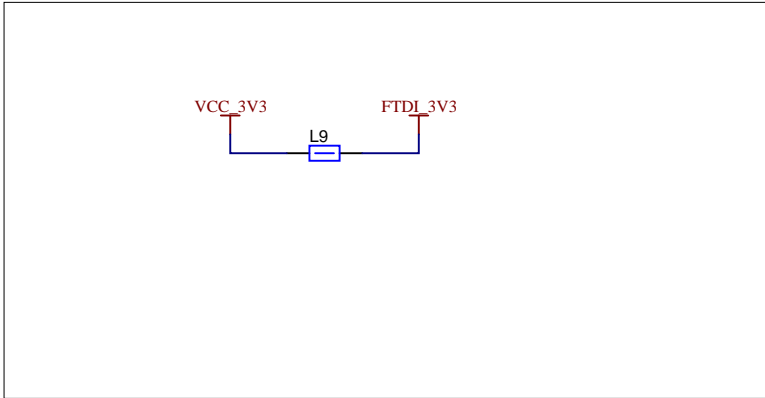
## DECOUPLING CAPACITORS - XDS110



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Orderable: BP-IWRL6432WMOD	Designed for: Public Release	Mod. Date: 22-10-2025
TID #: N/A	Project Title: BP-IWRL6432WMOD	
Number: PROC212	Rev: A	Sheet Title: XDS110_INTERFACE
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 11 of 15
Drawn By: Mistral	File: PROC212A_XDS110_Interface.SchDoc	Size: B
Engineer: Mistral	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

FTDI - USB to SPI CONVERTER

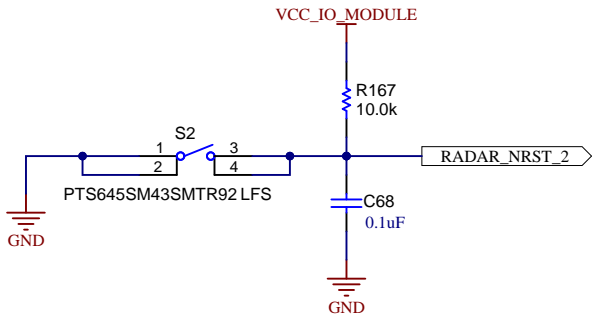


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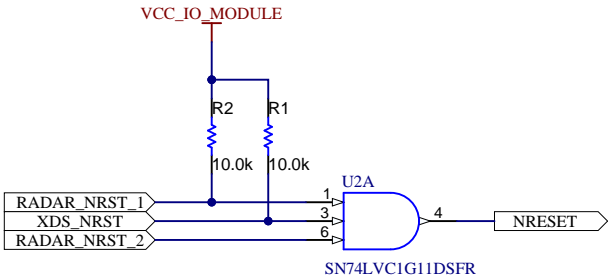
Orderable: BP-IWRL6432WMOD	Designed for: Public Release	Mod. Date: 22-10-2025
TID #: N/A	Project Title: BP-IWRL6432WMOD	
Number: PROC212	Rev: A	Sheet Title: FTDI_USB to SPI/I2C/UART converter
SVN Rev: Not in version control	Assembly Variant: 001_IWR	Sheet: 12 of 15
Drawn By: Mistral	File: PROC212A_FTDI.SchDoc	Size: B
Engineer: Mistral	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	

RESET SWITCH, LED & PRESENCE INDICATION LED

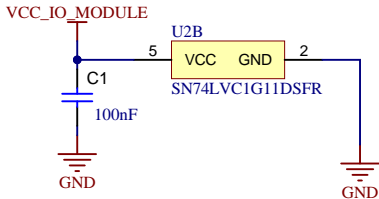
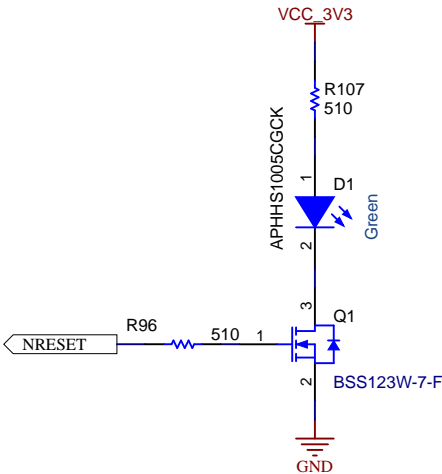
RESET SWITCH



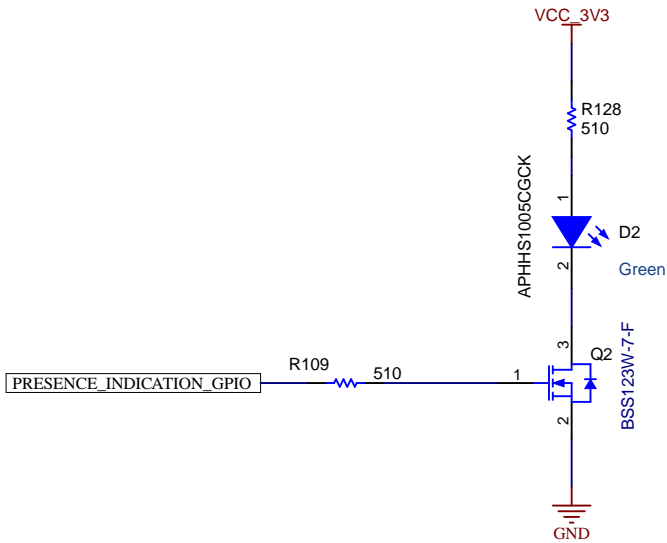
RESET SECTION



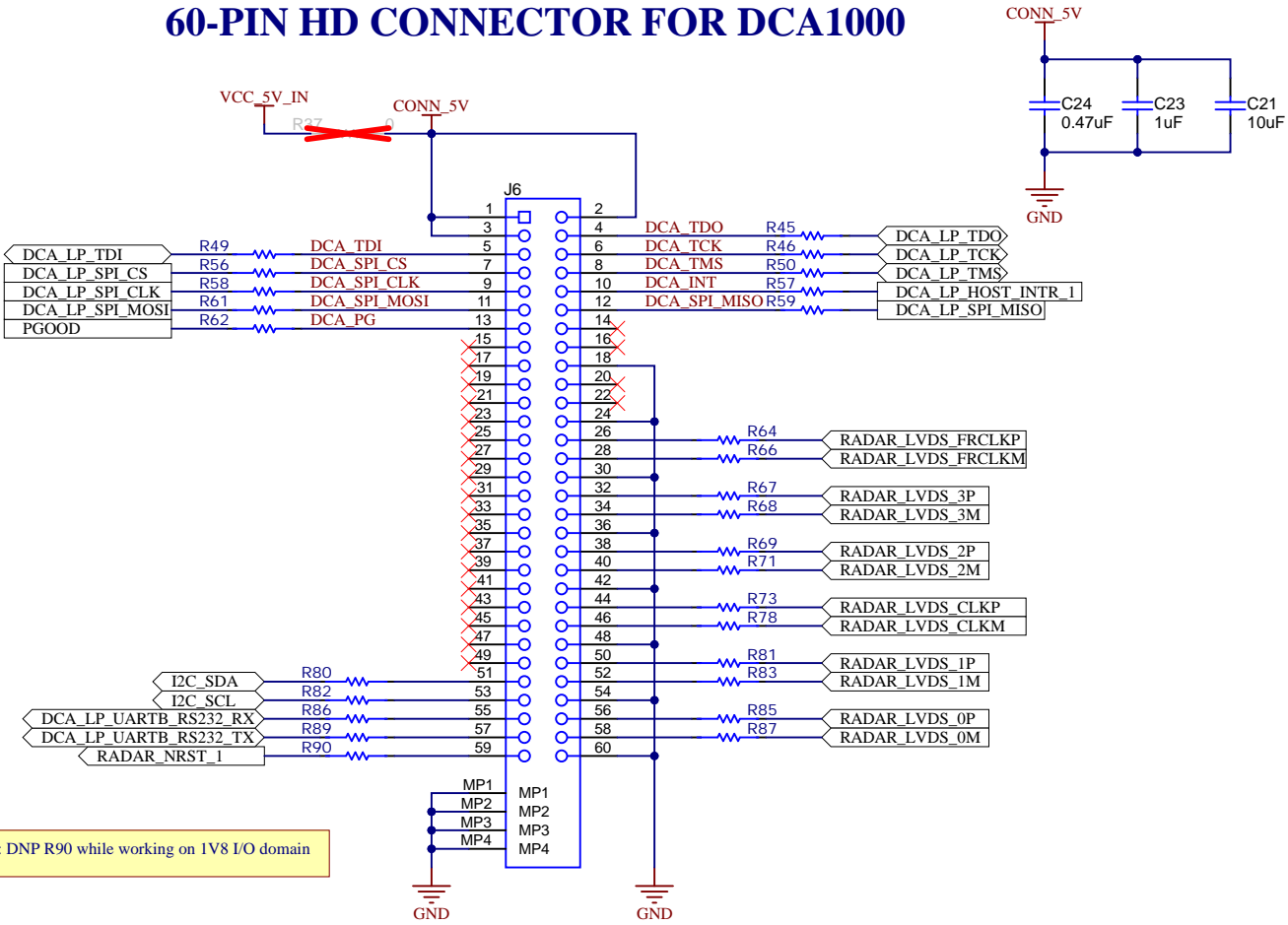
RESET LED



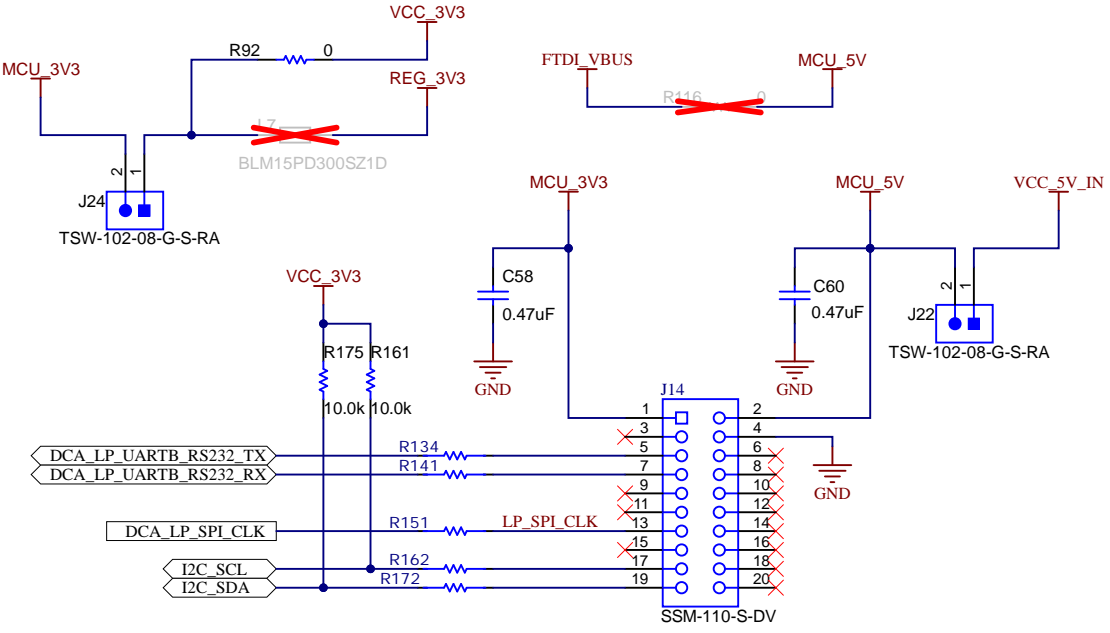
PRESENCE INDICATION LED



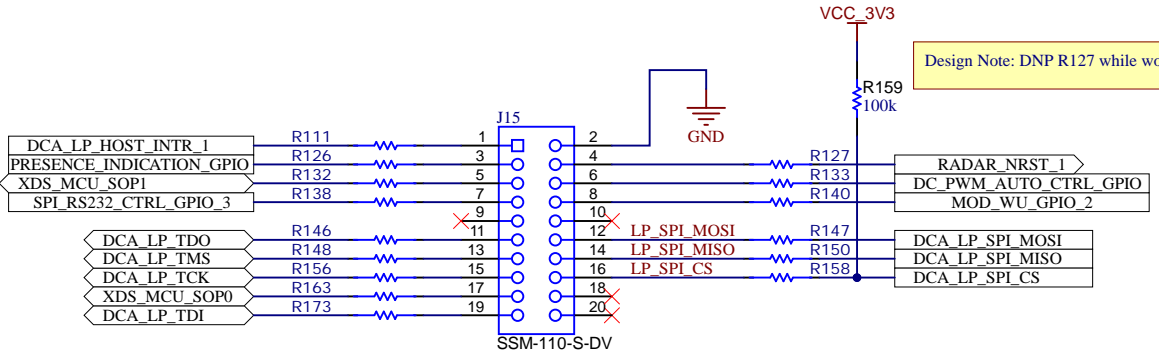
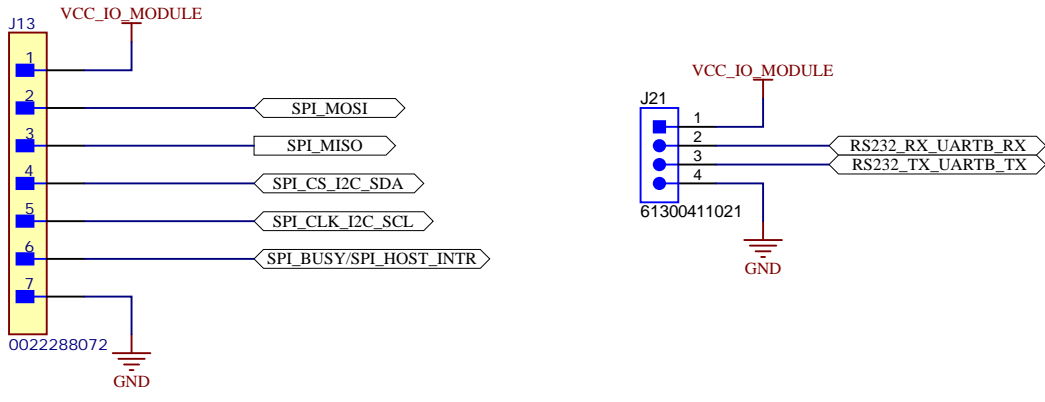
60-PIN HD CONNECTOR FOR DCA1000



LP-BP CONNECTOR



RS232, SPI CONN





PCB Number: PROC212  
PCB Rev: A

PCB  
LOGO  
Texas Instruments



PCB  
LOGO  
FCC disclaimer

PCB  
LOGO  
WEEE logo

CAUTION HOT SURFACE1



CAUTION HOT SURFACE

Variant/Label Table	
Variant	Label Text
001_IWR	BP-IWRL6432WMOD

LBL1

PCB Label

THT-14-423-10  
Size: 0.65" x 0.20 "

CAPACITORS HIGHLIGHTED IN THE RED COLOR BOXES ARE ADDED FOR IMPROVEMENT AND THOSE ARE NOT MANDITORY.

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

ZZ2

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ5

Assembly Note

INDICATION FOR COMPONENTS D\* ARE GIVEN AT THEIR CATHODE SIDE.

Orderable: BP-IWRL6432WMOD		Designed for: Public Release	Mod. Date: 22-10-2025
TID #: N/A		Project Title: BP-IWRL6432WMOD	
Number: PROC212	Rev: A	Sheet Title: HARDWARE	
SVN Rev: Not in version control		Assembly Variant: 001_IWR	Sheet: 15 of 15
Drawn By: Mistral		File: PROC212A_EVM_Hardware.SchDoc	Size: B
Engineer: Mistral		Contact: http://www.ti.com/support	